KBOC BASEBOARD#1 USER INFORMATION

KBOC_BB1_USER.PDF
KwikByte, LLC

Version 1.0

Revision Information

Revision	Date	Description
1.0	5/15/2009	Initial creation

DISCLAIMER

The KBOC_BB1 is an evaluation board intended for use in engineering development or demonstration and is not considered a final, end-item production unit. The device generates and uses radio frequency energy and has not been tested for compliance with FCC rules part 15. Use and operation of this device may cause radio interference – in which case the user must take corrective action at his own expense. In most cases, this simply involves discontinuing use of the device in that particular environment. Manufacturer is under no obligation to continue to produce this equipment for any length of time. This product is not intended for use in life-sustaining or life-critical systems. This product is not intended for use in nuclear devices. Appropriate ESD handling precautions must be taken when handling the device.

1 Introduction

The KBOC BASEBOARD#1 is intended for use as a hardware interface to the OMAP35xx-based KBOC System Module. This document provides important information about the KBOC BASEBOARD#1 ("KBOC_BB1") including physical dimensions, connector location and pin-out, and peripheral signal routing.

1.1 Physical Details

The figure below shows the KBOC_BB1 physical dimensions (7.00" x 4.50") and connector placement.

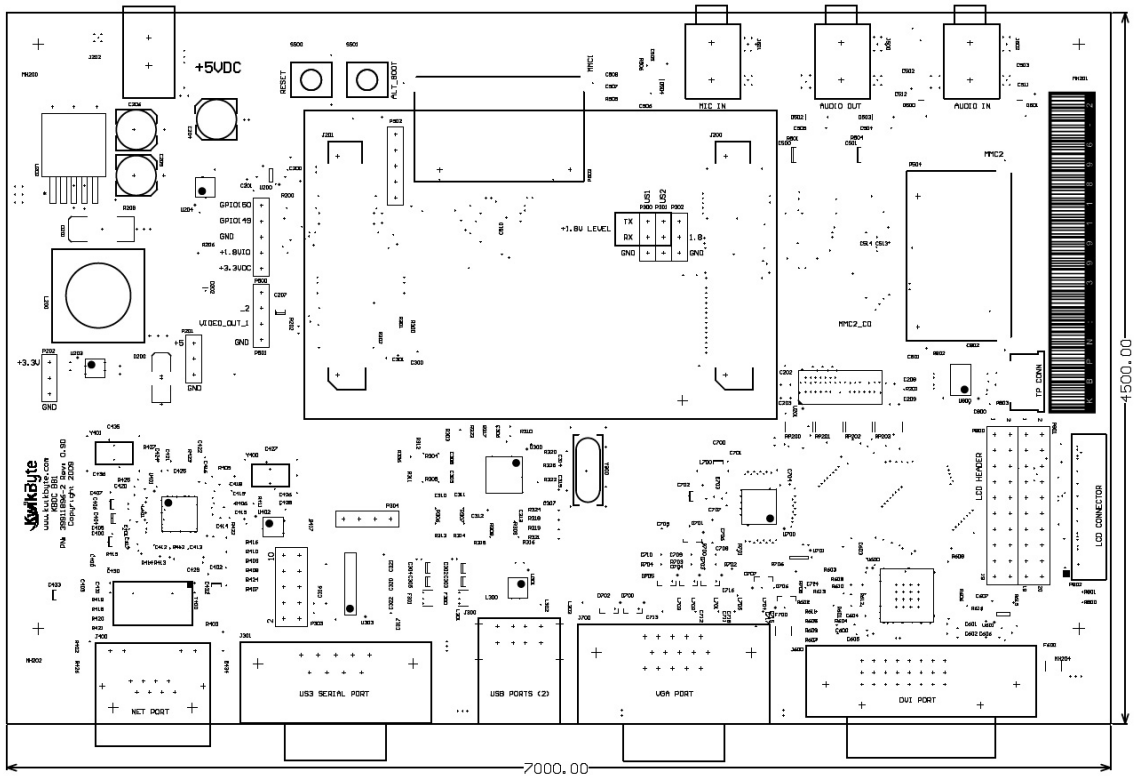

Figure 1-1: KBOC_BB1 DIMENSIONS

The figures below depict 3D images of the board viewed from top and connector edges. Note: some components shown are populated depending on configuration and may not be installed on a specific board.

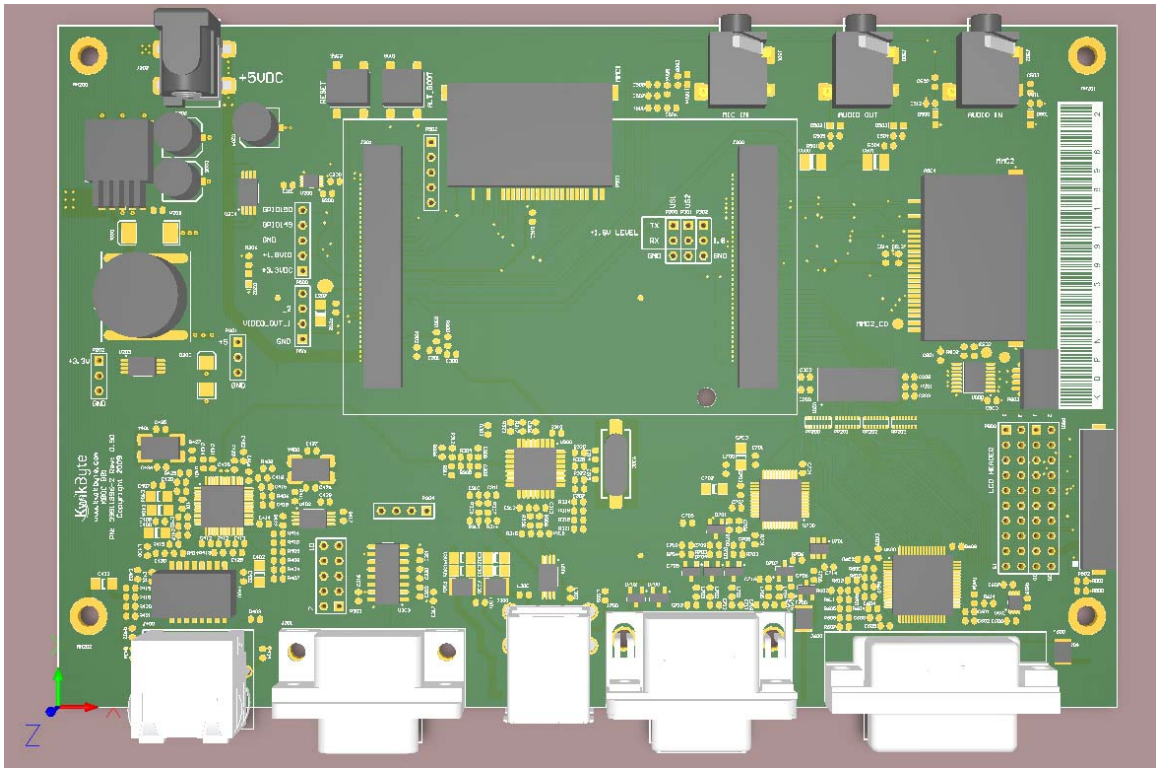

Figure 1-2: KBOC_BB1 3D VIEW FROM TOP

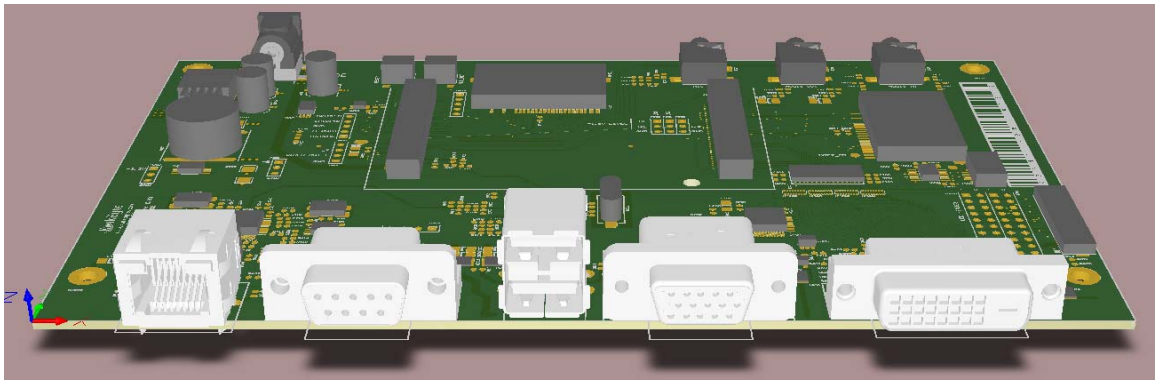

Figure 1-3: KBOC_BB1 3D VIEW FROM FRONT

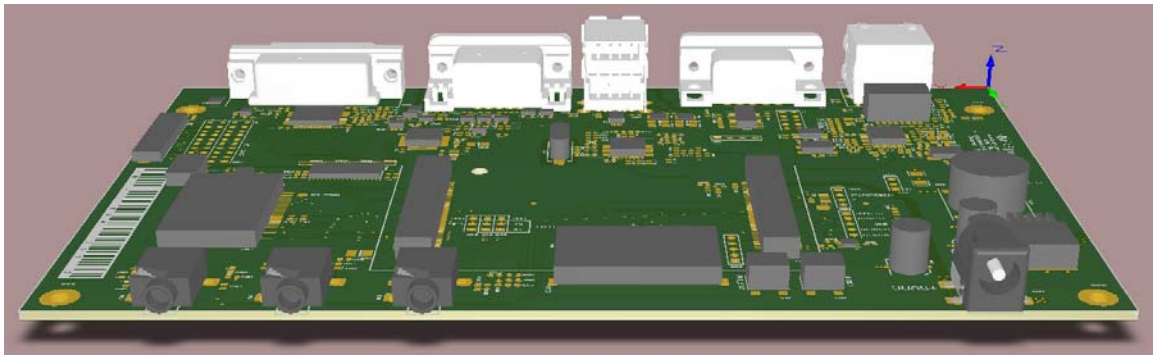

Figure 1-4: KBOC_BB1 3D VIEW FROM BACK

1.2 Connector Location and Pin-Out

The figure below shows the KBOC_BB1 with all connectors and headers labeled.

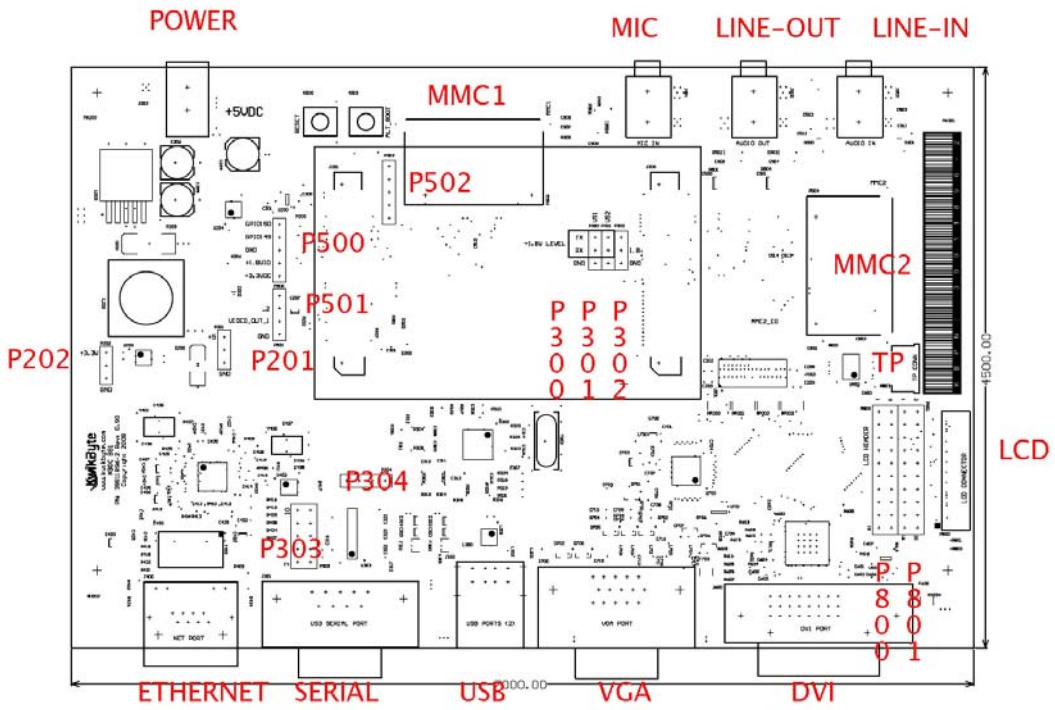

Figure 1-5: KBOC_BB1 CONNECTOR/HEADER LABELS

1.2.1 Connector Description

The list below describes each card-edge connector.

POWER:
Input power supply. Standard 2.1mm barrel jack, center-positive supply must be supplied with +5VDC. Current rating depends on application. This positive supply signal is called “DC_5V”.

MMC1:
Standard SD/MMC/mini SD/ micro SD connector. Typically used for mass-storage support.

MIC:
Not normally populated. This is electret type microphone input.

LINE-OUT:
Audio output at line level – 3.5mm stereo jack.

LINE-IN:
Audio input at line level – 3.5mm stereo jack.

MMC2:
Not normally populated.

TP:
4-wire resistive touch screen surface mount 1mm interface connector. Only installed on LCD versions.

LCD:
40-pin surface mount 0.5mm pitch LCD FPC connector. Only installed on LCD versions.

DVI:
Standard DVI video output connector.

VGA:
Standard VGA video output connector.

USB:
Dual, USB 2.0 FS host ports.

SERIAL:
RS232 serial connector (DB9 female) for channel USART3. This channel is typically used as the console port, although it can be used for other purposes. Pin 2 (RX) is an input relative to the processor. Pin 3 (TX) is an output relative to the processor. Pin 5 is signal ground.

ETHERNET:
Standard 10/100Mbps Ethernet jack.

1.2.2 Header Pin-out

The tables below describe the header pin-out information. The headers are standard, 0.100” x 0.100” through-hole headers that are not populated. This makes soldering to the signals very easy.

PIN	SIGNAL
1	DC_5V
2	NC
3	GND

Table 1-1: P201 Pin-out

PIN	SIGNAL
1	+3.3VDC
2	NC
3	GND

Table 1-2: P202 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	US1_TX	AA8
2	US1_RX	Y8
3	GND	

Table 1-3: P300 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	US2_TX (MCBSP3_CLKX)	AF5
2	US2_RX (MCBSP3_FSX)	AE5
3	GND	

Table 1-4: P301 Pin-out

PIN	SIGNAL
1	+3.3VDC
2	VIO_1V8
3	GND

Table 1-5: P302 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	NC	
2	UART3_232RX	H20 (RS232-LEVEL)
3	UART3_232TX	H21 (RS232-LEVEL)
4	NC	
5	GND	
6	NC	
7	NC	
8	NC	
9	NC	
10	NC	

Table 1-6: P303 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	NC	
2	GND	
3	US3_3.3V_RX	H20 (3.3V-LEVEL)
4	US3_3.3V_TX	H21 (3.3V-LEVEL)

Table 1-7: P304 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	+3.3VDC	
2	VIO_1V8	
3	GND	
4	LED1_GPIO149	AA9
5	LED1_GPIO150	W8

Table 1-8: P500 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	GND	
2	VIDEO_OUT1	Y28
3	VIDEO_OUT2	W28
4	GND	

Table 1-9: P501 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	SPI3_SOMI (USB1_DAT1)	AG12
2	SPI3_SIMO (USB1_DAT0)	AF11
3	SPI3_CS0 (USB1_DAT2)	AH12
4	SPI3_CLK (USB1_DAT3)	AH14
5	GND	

Table 1-10: P502 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	DD0	AG22*
2	DD15	AA27*
3	DD14	AA28*
4	DD12	AB28*
5	DD11	AD27*
6	DD10	AD28*
7	DD23	AC28*
8	DD21	J26*
9	DD18	H26*
10	DD17	H27*
11	DD1	AH22*
12	DD2	AG23*
13	DD5	AH24*
14	DD13	AB27*
15	GND	
16	GND	
17	DD_CK	D28*
18	DD_EN	E27*
19	DD_HS	D26*
20	DD_VS	D27*

Table 1-11: P800 Pin-out

* All display lines are buffered and driven at +3.3V level outputs.

PIN	SIGNAL	OMAP35xx BALL
1	LCD_PWR_ENn	Y21* (MCBSP1_CLKR)
2	LCD_PUP	V21* (MCBSP1_DX)
3	+3.3VDC	
4	+3.3VDC	
5	DD9	G26*
6	DD8	F27*
7	DD20	E28*
8	DD19	H25*
9	DD16	G25*
10	DD22	AC27*
11	DD3	AH23*
12	DD4	AG24*
13	DD7	F28*
14	DD6	E26*
15	GND	
16	GND	
17	I2C3_SCL	AF14 (DC_5V LEVEL)
18	DC_5V	
19	I2C3_SDA	AG14 (DC_5V LEVEL)
20	DC_5V	

Table 1-12: P801 Pin-out

1.3 On-Board Signal Routing

The lists below describe signals used on-board.

Ethernet Chip Reset Signal:
Active low reset, +3.3V signal.
ETH_RESETn : GPIO13 (USB1_CLK) : AE10 : Mode 4 0x25DA

USB Hub Reset Signal:
Active low reset, +3.3V signal.
USB_HUB_RESETn = GPIO22 (USB1_DIR) : AF9 : Mode 4 0x25EC

VGA Enable Signal:
Active low reset, +3.3V signal.
VGA_PUP = GPIO159 (MCBSP1_DR) : U21 : Mode 4 0x2192

DVI Enable Signal:
Active low reset, +3.3V signal.
DVI_PUP = GPIO170 : J25 : Mode 4 0x216C

LCD Enable Signal:
Buffered output driven at +3.3V level to header P801 pin 2.
LCD_PUP = GPIO158 (MCBSP1_DX) : V21 : Mode 4 0x2190

LCD Power Enable Signal:

Buffered output driven at +3.3V level to header P801 pin 1.
LCD_PWR_ENn = GPIO156 (MCBSP1_CLKR) : Y21 : Mode 4 0x218C

Touch Screen Interface Signals:
SPI1_CLK : AB3 : Mode 0
SPI1_CS3 : AB2 : Mode 0
SPI1_SIMO : AB4 : Mode 0
SPI1_SOMI : AA4 : Mode 0
IRQ = GPIO161 (MCBSP1_FSX) : K26 : Mode 4 0x2196

Monitor Detect Signals:
Buffered bidirectional signals driven at DC_5V level routed to header P801, DVI connector, and VGA connector.
I2C3_SCL = AF14 : Mode 0
I2C3_SDA = AG14 : Mode 0

Serial Channel 3 Signals:
Buffered +3.3V signals wired to header P304 and serial level shift chip, then wired to connector J301 and header P303.
US3_TX = H21 : Mode 0
US3_RX = H20 : Mode 0